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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/772,986	01/31/2001	Hisao Hayashi	SON-2010	2637

7590 10/06/2004

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EXAMINER	
TRAN, THIEN F	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/06/2004

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/772,986
Filing Date: January 31, 2001
Appellant(s): HAYASHI ET AL.

Ronald P. Kananen
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 07/07/2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1, 3 and 13, claim 2, claim 4, claims 5, 7 and 15, claim 6, claim 8, claim 14, and claim 16 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

Hisao Hayashi et al. "Thin Film Semiconductor Device" Japanese Kokai Patent Application No. HEI 10-209467 (Aug 7, 1998).

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8, 13 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Hisao et al. (JP 10-209467).

Hisao et al. discloses the claimed display device (Fig. 6) comprising an insulating substrate 1; pixels 14 arranged in a matrix form; and thin film transistors 3 (Fig. 1) for driving said respective pixels, wherein said pixels and said thin film transistors are formed as integrated circuits on said insulating substrate, each of said thin film transistors has a bottom gate structure having a gate electrode 5, a gate insulating film 4 and a semiconductor thin film 2 stacked in the order from below upward, and said gate electrode 5 is made of metallic material having an upper layer 5a of about 50-300 nm and a lower layer 5b of 50-200 nm (see Figures 1 and 2A, paragraph [0012]) that together provides a gate combined thickness of about 100 nm to 500 nm. Hisao et al. discloses said gate electrode 5 having a thickness of about 100 nm which allows for thickness slightly above or less than 100 nm, such as 99.99 nm. Hisao et al. further discloses said gate insulating film 4 has a film thickness in the range of 100-200 nm. Therefore, a thickness of 110 nm from the disclosed range for the gate insulating film 4,

and a thickness of less than 100 nm, i.e. 99.99 nm, for the gate electrode (5a, 5b) meet the claim limitations.

Regarding claims 3 and 7, said semiconductor thin film 2 comprises polycrystalline silicon crystallized by an irradiation of a laser beam.

Regarding claims 4 and 8, said gate electrode has a multi-layer structure stacked with an upper layer 5a having comparatively low heat conductivity and high electric resistance (inherent characteristic), and a lower layer 5b having comparatively high heat conductivity and low electric resistance (see paragraph [0012]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hisao et al. (JP 10-209467).

Hisao et al. as described above discloses the gate electrode having a thickness of about 100 nm (slightly less than 100 nm) but does not specifically disclose the thickness of the gate electrode being 90 nm. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form the gate electrode having a thickness of 90 nm to reduce the size of the device as small as possible, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only

routine skill in the art. In re Aller, 105 USPQ 233. In re Daily, 93 USPQ 47 (CCPA 1966), the court held that changes in size and shape of parts of an invention in the absence of an unexpected result involve routine skill in the art. Additionally, In Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device. Indeed, Hisao discloses the same structure with the gate thickness of 99.99 nm that is capable of providing the same advantage as the gate thickness of 90 nm since Appellant clearly discloses a gate electrode having a gate thickness of less than 100 nm (including 99.99 nm and 90 nm) would provide the same advantage, reducing the thermal capacity of the gate electrode. Therefore, the claimed gate thickness of 90 nm would not perform differently than the prior art device.

(11) Response to Argument

Regarding claims 1-3, 13 and claims 5-7 and 15, Appellant argues that the office action fails to show that Hisao teaches a gate electrode 5 having a thickness of less than 100 nm and the gate insulating film 4 having a thickness that is greater the thickness of the gate electrode 5 of Hisao. The examiner respectfully disagrees with the remark because Hisao clearly teaches the combined thickness of layers 5a and 5b of the gate electrode 5 being about 100 nm which allows for a gate thickness near or approximately 100 nm. Therefore, a gate thickness of 99.99 nm of the gate electrode 5

clearly meets the claim limitation that requires a gate electrode having a thickness of less than 100 nm. Hisao further discloses a gate insulating film 4 having a thickness of 100-200 nm. Therefore, a selected thickness of 110 nm for the gate insulating film 4 from the disclosed range is greater than the thickness of the gate electrode 5 of 99.99 nm.

Regarding claims 4 and 8, Appellant argues that the office action fails to show that the upper layer 5a of Hisao has comparatively low heat conductivity and high electric resistance, and that the lower layer 5b of Hisao has comparatively high heat conductivity and low electric resistance. The examiner respectfully disagrees with the remark because Hisao clearly teaches the top layer 5a having relatively low thermal conductivity and the bottom layer 5b having relatively high thermal conductivity and low resistance (paragraph [0012]). Hisao further discloses the top layer 5a being formed of ITO film, TiN film or TiON film which are materials known to have high electric resistance (inherent characteristic) compared with metal film, e.g., W, Cr, Mo, or Ti used as materials for the bottom layer 5b. It is a fact that ITO, TiN or TiON are materials that possess high electric resistance characteristic as compared with metals, such as W, Ti, Cr or Mo and Appellant fails in producing evidence to support his contention that ITO, TiN or TiON do not have high electric resistance characteristic as compared with W, Ti, Cr, or Mo. It is elementary that the mere recitation of a newly discovered function or property, inherently possessed by things in the prior art, does not cause a claim drawn to distinguish over the prior art. Additionally, where the Patent Office has reason to believe that a functional limitation asserted to be critical for establishing novelty in the

claimed subject matter may, in fact, be an inherent characteristic of the prior art, it possesses the authority to require the applicant to prove that the subject matter shown to be in the prior art does not possess the characteristic relied on. In re Swinehart, 169 USPQ 226 (CCPA 1971). See also, In re Ludtke, 441 F.2d 660, 169 USPQ 563 (CCPA 1971) and In re Fitzgerald, 619 F.2d 67, 205 USPQ 594 (CCPA 1980).

Regarding claims 14 and 16, Appellant argues that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). Also, it is obvious as described in appellant's specification that the gate thickness of 99.99 nm and 90 nm would provide the same advantage. Therefore, it is obvious to make the gate thickness as small as possible by selecting a gate thickness of 90 nm since the gate thickness is variable of importance subject to routine experimentation and optimization. It is quite clear that the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.

In conclusion, it is respectfully submitted that a prima facie case of anticipation and obviousness have been established and that Appellant has failed to rebut.

For the above reasons, it is believed that the rejections should be sustained.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

tt
September 27, 2004

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PRIMARY EXAMINER

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Alexandria, Virginia 22313-1450

09/772,986

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.

EXAMINER	
ART UNIT	PAPER
	09272004

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

Copies of English language translation of Japanese reference 10-209467 were obtained from STIC Translations Branch and forwarded to the Board of Patent Appeals and Interferences for consideration. Also, a copy of translation is hereby provided to Applicant.

PTO 04-2050

Japanese Kokai Patent Application
No. 10[Hei]-209467

THIN FILM SEMICONDUCTOR DEVICE

Hisao Hayashi and Ken Shimokakiuchi

UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. MARCH 2004
TRANSLATED BY THE RALPH MCELROY TRANSLATION COMPANY

JAPAN PATENT AND TRADEMARK OFFICE (JP)
PATENT JOURNAL (A)
KOKAI PATENT APPLICATION NO. HEI 10[1998]-209467

Int Cl.[6]:	H 01 L 29/786 G 02 F 1/136 H 01 L 21/20 21/336 29/78
Filing No.:	Hei 09[1997]-026184
Filing Date:	January 24, 1997
Publication Date:	August 7, 1998
No. of Claims:	6 (9 pages in total; FD)
Examination Request:	Not filed

THIN FILM SEMICONDUCTOR DEVICE

[Usumaku handotai sochi]

Inventor	Hisao Hayashi and Ken Shimokakiuchi
Applicant	000002185 Sony Corp.

[Abstract]

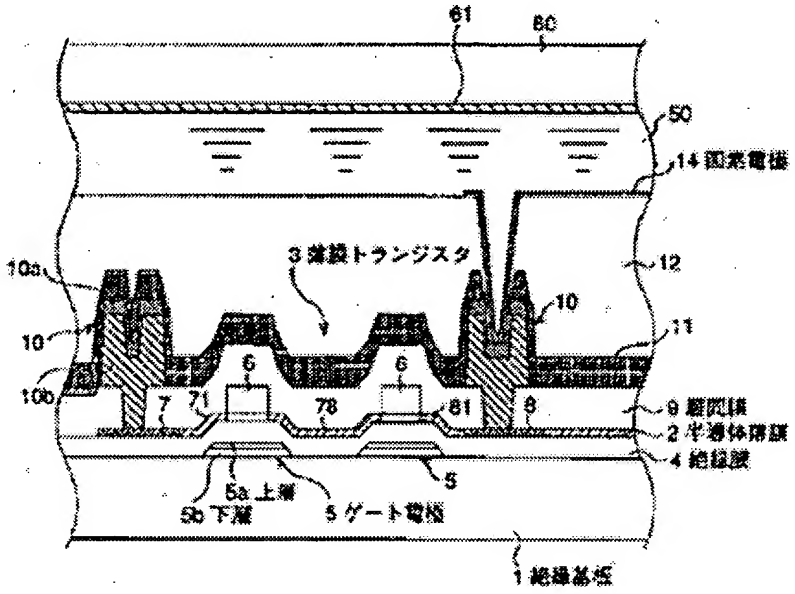
Problem

To optimize and make more uniform the recrystallization treatment by laser annealing of semiconductor thin films that comprise the active layer in bottom-gate type thin film transistors.

Means of Solution

Thin film semiconductor devices are formed by laminating thin film transistors 3 on an insulating substrate 1. Thin film transistors 3 have a bottom-gate structure in which a gate electrode 5, an insulating layer 4, and a semiconductor thin film 2 are laminated in order from the bottom up. The gate electrode 5 possesses a multilayered structure in which a top layer 5a

equipped with relatively low thermal conductivity and electrical conductivity necessary to form contacts is laminated with a bottom layer 5b equipped with relatively high thermal conductivity and electrical conductivity necessary to function as wiring. The semiconductor thin film 2 extends over the gate electrodes 5 and insulating substrate 1 with an interceding insulating film 4, and manifests a polycrystalline structure that has been uniformly and optimally recrystallized by energy irradiation. Depending on the circumstances, a thermally conductive base film may be formed on the surface of the insulating substrate 1 so as to be adjacent to the gate electrodes 5, when viewed from the top, to make the thermal conductivity of the surface of the insulating substrate 1 more uniform.



Key:
	1	Insulating Substrate
	2	Semiconductor Thin Film
	3	Thin Film Transistor
	4	Insulating Film
	5	Gate Electrode
	5a	Top Layer
	5b	Bottom Layer
	9	Interlayer Film
	14	Pixel Electrode

Claims

1. A thin film semiconductor device in which a thin film transistor with a bottom-gate structure, comprising gate electrodes, an insulating film, and a semiconductor thin film laminated in order from the bottom up, is formed aggregated on an insulating substrate, which thin film semiconductor is characterized by the aforementioned gate electrodes each possessing a

multilayered structure in which a top layer with relatively low thermal conductivity and electrical conductivity necessary to form contacts is laminated with a bottom layer with relatively high thermal conductivity and electrical conductivity necessary to function as wiring, and by the aforementioned semiconductor thin film possessing a polycrystalline structure, which has been recrystallized by energy irradiation, extending over said gate electrodes and said insulating substrate with an interceding insulating film.

2. The thin film semiconductor device disclosed in Claim 1, which is characterized by the aforementioned gate electrodes having a trapezoidal sectional profile.

3. The thin film semiconductor device disclosed in Claim 1, which is characterized by at least one or the other of the top layer or bottom layer of the aforementioned gate electrodes having light-blocking properties.

4. A thin film semiconductor device in which a thin film transistor with a bottom-gate structure, comprising gate electrodes, an insulating film, and a semiconductor thin film laminated in order from the bottom up, is formed aggregated on an insulating substrate, which thin film semiconductor is characterized by forming a thermally conductive base on the surface of the insulating substrate so as to be adjacent to the gate electrodes, when viewed from the top, to make the thermal conductivity of the surface of the insulating substrate more uniform, and by the aforementioned semiconductor thin film possessing a polycrystalline structure, which has been recrystallized by energy irradiation, extending over said gate electrodes and said base film with an interceding insulating film.

5. A display device that is equipped with a pair of insulating substrates bonded together with an intervening specified gap and an electrooptical substance held in said gap, and in which a pair of electrodes is formed on one of the insulating substrates and a thin film transistor with a bottom-gate structure, comprising gate electrodes, an insulating film, and a semiconductor thin film laminated in order from the bottom up, and pixel electrodes are formed aggregated on the other insulating substrates, which display device is characterized by the aforementioned gate electrodes each possessing a multilayered structure in which a top layer with relatively low thermal conductivity and electrical conductivity necessary to form contacts is laminated with a bottom layer with relatively high thermal conductivity and electrical conductivity necessary to function as wiring, and by the aforementioned semiconductor thin film possessing a polycrystalline structure, which has been recrystallized by energy irradiation, extending over said gate electrodes and said insulating substrate with an interceding insulating film.

6. A display device that is equipped with a pair of insulating substrates bonded together with an intervening specified gap and an electrooptical substance held in said gap, and in which a pair of electrodes is formed on one of the insulating substrates and a thin film transistor with a bottom-gate structure, comprising gate electrodes, an insulating film, and a semiconductor thin

film laminated in order from the bottom up, and pixel electrodes are formed aggregated on the other of the insulating substrates, which display device is characterized by forming a thermally conductive base on the surface of the other of the insulating substrates so as to be adjacent to the gate electrodes, when viewed from the top, to make the thermal conductivity of the surface of the insulating substrate more uniform, and by the aforementioned semiconductor thin film possessing a polycrystalline structure, which has been recrystallized by energy irradiation, extending over said gate electrodes and said base film with an interceding insulating film.

Detailed explanation of the invention

[0001]

Industrial application field

This invention pertains to a thin film semiconductor device in which a bottom-gate type thin film transistor, with a polycrystalline silicon, etc. active layer, is formed aggregated on an insulating substrate. More specifically, it pertains to the manufacture of a polysilicon thin film transistor produced by a low-temperature process at 600°C or lower.

[0002]

Prior art

Thin film semiconductors are optimal as driver substrates for use as active matrix liquid crystal displays, and there recently has been extensive progress in their development. Polycrystalline silicon or amorphous silicon is used in the active layer of thin film transistors. In particular, polycrystalline silicon thin film transistors have been successfully applied to miniature, high-precision active matrix color liquid crystal display devices and have been gaining attention. Polycrystalline silicon thin films, actively used only as electrode materials or resistor materials in conventional semiconductor technology, are a technology that is employed as active layers to form thin film transistors as pixel switching elements on insulating substrates made from transparent glass, etc. It is the only technology capable of realizing thin film transistors for the high-performance switching elements that can be used in the high-density design necessary to realize the video components demanded by the market. At the same time, it has also made it possible to form peripheral circuits that use conventional outboard IC units on the same substrate and at the same time as the pixel elements. This makes it possible to realize the high-precision active matrix liquid crystal displays together with their peripheral circuits that could not be realized with amorphous silicon thin film transistors.

[0003]

Since polycrystalline silicon has greater carrier mobility than amorphous silicon, polycrystalline silicon thin film transistors have a higher current drive capacity, and the peripheral circuits that require high-speed drive, e.g., horizontal scanning circuits and vertical scanning circuits, etc., can be simultaneously formed on the same substrate as the thin film transistors used for pixel switching. Consequently, the number of signal lines used to transmit outside the display thin film semiconductor device can be vastly reduced. In addition, CMOS circuits formed by laminating N-channel and P-channel thin film transistors can be brought on-chip and built into level shift circuits, and timing system signals can be driven at lower voltages.

[0004]

High-temperature process technologies that utilize process temperatures of 1,000°C and higher were established in the past as device technologies and process technologies in thin film transistors. One feature of these high-temperature processes is the reformation by solid phase growth of the semiconductor thin film formed on a high-temperature resistant substrate, such as quartz. Solid phase growth is a method in which the semiconductor thin film is heat-treated in the film formation stage at a temperature of 1,000°C or higher, to increase size of the individual crystal grains contained in the polycrystalline silicon, which is an aggregation of minute silicon crystals. Polycrystalline silicon obtained by this solid phase growth method yields high carrier mobility on the order of 100 $cm^2/v.s$. It is essential to use a substrate of superior heat resistance to implement this kind of high-temperature process, and high-quality quartz and the like has been used in the past. However, quartz has a disadvantage from the viewpoint of decreasing manufacturing costs.

[0005]

Low-temperature processes that utilize lower processing temperatures of 600°C or lower have been developed to replace the high-temperature processes described above. Laser annealing, which uses a laser beam, has gained some attention as a part of the conversion of the thin film semiconductor device manufacturing process to a lower temperature process. This method shines a laser beam to locally heat a melt a non-monocrystalline semiconductor thin film, amorphous silicon film or polycrystalline silicon film that has been formed on a low-heat resistance insulating substrate, such as glass, and then crystallizes the semiconductor thin film by a cooling process. These crystallized semiconductor thin films are then laminated as active layers (channel regions) to form polycrystalline silicon thin film transistors. Since the carrier mobility

of crystallized semiconductor thin film is increased, the performance of the thin film transistors can be increased to some extent.

[0006]

Incidentally, the mainstream structure for thin film transistors is conventionally a top-gate structure. In a top-gate structure, a semiconductor thin film is formed on top of an insulating substrate, and then gate electrodes are formed on top, with an interceding gate insulating film. Low-cost, large-scale glass plates are used as the insulating substrates in low-temperature processes. Since these glass plates contain large quantities of metal impurities, such as Na, etc., the Na, etc., will become localized according to the voltage used to drive the thin film transistors. The fluctuation of thin film transistor properties due to these electrical fields poses a reliability problem. In contrast, bottom-gate structures have been developed in recent years that are more suited to low-temperature processes. These are formed by disposing gate electrodes made from metal film, etc. on an insulating substrate, such as glass plate, and then forming a semiconductor thin film on top of these with an interceding gate insulating film. The gate electrodes have the effect of blocking the electrical charges in the glass plate, so that the bottom-gate structure is superior to the top-gate structure in terms of reliability from a structural viewpoint. In this connection, data comparing the reliability of bottom-gate and top-gate thin film transistors are shown in Figure 7. These data were obtained by producing a CMOS ring oscillator with thin film transistors and chronologically measuring changes in the oscillation frequency at 120°C. As is clear from the graph in Figure 7, the operation properties are more stable in the bottom-gate structure than in the top-gate.

[0007]

Problems to be solved

However, bottom-gate structures have a significant problem when performing recrystallization by laser annealing. As a rule, the areas that are to become channel regions in the recrystallized semiconductor thin film are located directly above the gate electrodes, while the areas that are to become source regions and drain regions are on the glass substrate. Because of this, when energy is applied by laser beam irradiation, differences arise in the heat conduction and dissipation in the glass plate and in the metal gate electrodes. As a result, since the optimal laser energy differs for the channel regions and for the source regions and drain regions, it becomes impossible to perform laser irradiation at the optimal energy for yielding high carrier mobility. In other words, when performing recrystallization by laser annealing, the laser beam is simultaneously applied on both the semiconductor thin film on the metal gate electrodes and on the semiconductor thin film on the glass plate, but since during the period in which the

semiconductor thin film is melted, cooled, and solidified, the heat on the metal gate electrodes is transferred to the gate wiring and dissipates horizontally, it solidifies in a relatively short time. Therefore, the crystal grains differ in the recrystallized semiconductor thin film over the metal gate electrodes from that over the glass plate, making its carrier mobility uneven. In the extreme, when attempting to increase the crystal grain size of the semiconductor thin film over the metal gate electrode, the irradiation energy will be become too high in the semiconductor thin film on the glass plate, vaporizing the thin film. Conversely, if trying to normalize the crystal state of the semiconductor thin film over the glass plate, the crystal grain size of the semiconductor thin film over the metal gate electrodes will be too small. This is the problem that is to be solved with conventional bottom-gate structures.

[0008]

Means to solve

The following means have been proposed to solve the problems in prior art described above. The basic structure of the thin film semiconductor device according to this invention is one in which gate electrodes, an insulating film, and a semiconductor thin film are laminated in order from the bottom up on an insulating substrate to form a bottom-gate thin film transistor structure. The characteristic item is that the aforementioned gate electrodes possess a multilayered structure with layering at least a top layer equipped with relatively low thermal conductivity and the electrical conductivity necessary to form contacts with a bottom layer equipped with relatively high thermal conductivity and electrical conductivity necessary to function as wiring. The aforementioned semiconductor thin film possesses a polycrystalline structure that has been recrystallized by energy irradiation that exists extending over said gate electrodes and said insulating substrate with said insulating film interceding. The aforementioned gate electrodes preferably have a trapezoidal sectional profile. Additionally, at least one of either the top or bottom layer of the aforementioned gate electrodes preferably has light-blocking properties.

[0009]

According to another aspect of this invention, a thin film semiconductor device in which a thin film transistor with a bottom-gate structure, comprising gate electrodes, an insulating film, and a semiconductor thin film laminated in order from the bottom up, is formed aggregated on an insulating substrate, is characterized by forming a thermally conductive base on the surface of the aforementioned insulating substrate so as to be adjacent to the gate electrodes, when viewed from the top, to make the thermal conductivity of the surface of the insulating substrate more uniform. In this case, the aforementioned semiconductor thin film possesses a polycrystalline

structure, which has been recrystallized by energy irradiation, and extends over said gate electrodes and said base film with said insulating film interceding.

[0010]

According to the first aspect of this invention, the laminated structure of the gate electrodes is formed with a top layer equipped with relatively low thermal conductivity and the electrical conductivity necessary to form contacts is formed as the laminated structure of the gate electrode. This minimizes the difference in the states of thermal conductivity over the gate electrodes and over the insulating substrate. This makes is possible to optimize the laser energy to facilitate obtaining a high-quality polycrystalline semiconductor thin film. In addition, it is common when the thermal conductivity is low for electrical conductivity to be correspondingly low. This is a disadvantageous condition for gate wiring. Therefore, by providing a bottom layer with the electrical conductivity necessary to function as wiring, this invention allows for decreased resistance. As described above, the thermal conductivity of the conductive material used as the gate electrodes may be decreased in order to even out distribution of heat across the entire surface of the insulating substrate. However, it is best to make the specific resistance of the gate wiring as low as possible. Because these two properties are contradictory, the gate electrodes in the first aspect of this invention have a two-layered structure utilizing upper and lower layers in which these properties are acceptable. In addition, in the second aspect of this invention, a thermally conductive base film is formed so as to be adjacent to the gate electrodes when viewed from above, in order to make the thermal conductivity uniform over the surface of the insulating substrate. Thus, it becomes possible to accomplish uniform recrystallization of the semiconductor thin film by laser annealing, and to optimize the laser beam irradiation conditions.

[0011]

Embodiments

Embodiment of this invention will be explained in detail below, using the attached figures. Figure 1 is a schematic partial cross-sectional drawing showing a first application example of the semiconductor thin film of this invention. As shown in this figure, this thin film semiconductor device has a thin film transistor 3 with a bottom-gate structure, in which a gate electrode 5, insulating film 4, and semiconductor thin film 2 are laminated in order from the bottom up, is formed accumulated on an insulating substrate 1, made from glass or the like. This thin film semiconductor device is used as the drive substrate for an active matrix display device. Therefore, a pixel electrode 14 is connected to the thin film transistor 3. In addition, the thin film transistor 3 has a double-gate structure to increase reliability. However, this invention is not limited to this and may of course be applied to single-gate structure thin film transistors, as well.

When assembling a display device, one insulating substrate 60 is bonded to another insulating substrate 1 with a specified interceding gap. The one insulating substrate 60 is made from glass, with opposing electrodes 61 already formed on its surface. The gap between the two substrates 60, 1 is maintained by an electrooptical substance, e.g., liquid crystal 50.

[0012]

A characteristic aspect of this invention is that the gate electrode 5 possesses a multilayered structure in which at least a top layer 5a and a bottom layer 5b are present. The top layer 5a is equipped with relatively low thermal conductivity and electrical conductivity necessary to form contacts. Typically, a compound film, e.g., ITO film, TiN film, or TiON film, etc., or an alloy metal film, e.g., nichrome, etc. is used. The thickness of this film is around 50 to 300 nm. On the other hand, the bottom layer 5b is equipped with relatively high thermal conductivity and electrical conductivity necessary to function as wiring. A low-resistance, high-melting point, metal film, e.g., W, Cr, Mo, or Ti, etc., is used. The thickness of this film is set in the range of 50 to 200 nm, e.g., 100 nm. The gate electrode 5 extends from gate wiring (not shown). Generally, the gate wiring has the same multilayered structure as the gate electrode 5 and is connected to other circuit components (not shown) through contact holes (not shown). In this relation, the top layer 5a has at least the electrical conductivity necessary to form contacts, and the bottom layer with the electrical conductivity necessary to function as wiring. The gate electrode has a trapezoidal sectional profile. The angle of the edge surfaces is 45° or less, preferably in the range of 5° to 15°. This trapezoidal shape is effective at preventing the film formed above the gate electrode 5 from shearing. In addition, at least on of the top layer 5a and bottom layer 5b of the gate electrode 5 has light-blocking properties, making the gate electrode 5 generally opaque. Thus, current leakage in the thin film transistor 3 due to incident light from the back of the insulating substrate 1, etc. can be controlled.

[0013]

The gate electrode 5 is covered with an insulating film 4 made from SiO_2, or the like. A semiconductor thin film 2 made from polycrystalline silicon, etc. is formed on top of the insulating film 4. Stoppers 6 are formed on the semiconductor thin film 2 by patterning to be aligned with each gate electrode 5. The portions of the semiconductor thin film 2 located immediately beneath each stopper 6 will become channel regions. Source regions 7 and drain regions, impregnated with high concentrations of impurities, are also formed in the semiconductor thin film 2. LDD regions 71, 78, 81, impregnated with low concentrations of impurities, are also formed. The thin film transistor 3 possessing this structure is then covered with an interstitial film 9 made from SiO_2, or the like. Signal wiring 10 is then formed by

patterning on top of the interstitial film 9 and electrically connected to the source region 7 of the thin film transistor 3 through contact holes. This signal wiring has a two-layered structure with a top metallic film 10a made from Mo or the like and a bottom metallic film 10b made from Al or the like. Wiring 10 is also formed by patterning to likewise connect to the drain region 8. This wiring 10 is covered by a smoothing film 12 with an interceding passivation film 11. A pixel electrode 14 made from ITO or the like is then formed on top of the smoothing film 12. This pixel electrode 14 is electrically connected to the drain region 8 of the thin film transistor 3 via a contact hole formed in the smoothing layer and connecting wiring 10.

[0014]

The method of manufacturing the thin film semiconductor device shown in Figure 1 will be explained in detail, referring to Figure 2. To simplify the figure, only one gate electrode is shown. First, as shown in (A), a bottom layer 5b is formed by sputtering over the entire surface of the insulating substrate 1, made from glass or the like. Since it is preferable that this bottom layer 5b have low resistance, and further desirable that it have a high melting point, a metal film such as W, Cr, Mo, or Ti, etc. is generally used. The film thickness is approximately 100 nm. The film thickness generally should be within the range of 50 to 200 nm. A top layer 5a is then consecutively or non-consecutively formed by sputtering over the entire surface of the bottom layer 5b. This top layer 5a is a characteristic element of this invention. The top layer 5a does not need to have low resistance, but a material with low thermal conductivity is used. Even though the top layer 5a is unsuitable as wiring, it must have the electrical conductivity necessary to form contacts. A compound film, e.g., an ITO film, TiN film, or TiON film, or alloy film, e.g., nichrome, is used as the top layer 5a. A relatively thick film thickness is better and is set in the range of about 50 to 300 nm.

[0015]

Next, as shown in (B), the multilayered film of the laminated top layer 5a and bottom layer 5b is patterned by, e.g., isotropic dry etching, to fabricate a gate electrode 5. The gate electrode 5 can be fabricated to a trapezoidal sectional profile by isotropic dry etching. In other words, the edge faces of the gate electrode 5 tapered to an angle in the range of 5° to 15°.

[0016]

As shown in (C), SiO_2 is accumulated to a thickness of 100 to 200 nm by plasma CVD (PE-CVD), to form an insulating film 4 covering the gate electrode 5. Furthermore, amorphous silicon is accumulated to a thickness of 20 to 60 nm to provide a semiconductor thin film 2. The insulating film 4 and semiconductor thin film 2 can be consecutively grown in the same film

formation chamber without breaking the vacuum. The insulating substrate is heated here to a temperature of, 400°C. An amorphous silicon semiconductor thin film 2 formed by PE-CVD has a hydrogen content of approximately 10% and this hydrogen is released by heat treatment at 400°C. Subsequently, irradiation with a 308 nm wavelength XeCl excimer laser provides for recrystallization of the semiconductor thin film 2. When the amorphous silicon is melted by the energy of the laser light and then solidifies, it becomes polycrystalline silicon. The crystallinity (primarily the crystal grain size) is determined by the time it takes for hardening to occur. Using a material of relatively low thermal conductivity as the top layer 5 of the gate electrode 5 in this invention minimizes horizontal dissipation of heat in this area and slows the speed at which it solidifies after melting. This yields polycrystalline silicon of sufficiently large grain size from the viewpoint of practicality. Since the gate electrode 5 is fabricated into a trapezoidal shape, it is possible to prevent the semiconductor thin film 2 from shearing at the stepped portions.

[0017]

As shown in (D), SiO_2 is accumulated by PE-CVD on top of the semiconductor thin film 2. The SiO_2 is patterned here using back-exposure technology to form a stopper 6. Namely, a stopper 6 that is aligned with the gate electrode 5 is obtained by self-alignment by performing back-exposure using the gate electrode 5, which has light-blocking properties, as a mask. The semiconductor thin film 2 is impregnated with impurities (e.g., phosphorous) to a relatively low concentration by ion doping, using the stopper as a mask. Furthermore, after covering the stopper and its perimeter with a photoresist, the semiconductor thin film 2 is impregnated by ion doping with impurities (e.g., phosphorous) to a relatively high concentration, thereby forming a source region 7 and drain region 8. Additionally, LDD regions 71, 81 with relatively low impurity concentrations are left in the areas of the semiconductor thin film covered by the resist. After this, the now unnecessary photoresist is removed. Ion doping dopes the semiconductor thin film 2 by field-accelerating ions in a plasma state all at once, so that the treatment can be performed in a short time.

[0018]

Finally, as shown in Figure (E), laser irradiation is performed again to activate the doped atoms. This is done by the same method as in recrystallization, but since the crystals do not need to be increased, a weaker energy level is adequate. SiO_2 is then accumulated to form an interstitial film 9 and provide insulation between wiring. After forming contact holes in the interstitial film 9, metallic aluminum or the like is then accumulated by sputtering and then patterned into a desired shape to fabricate wiring 10. Thereafter, when manufacturing a display

thin film semiconductor device, a passivation film, smoothing film, and pixel electrodes are formed as necessary.

[0019]

Figure 3 is a schematic representation of the temperature changes in the semiconductor thin film during laser annealing. In laser annealing pulsed excimer laser light is irradiated. With the pulsed irradiation, the temperature of the silicon (Si) that constitutes the semiconductor thin film sharply increases and exceeds its melting point. Then, after briefly maintaining a steady state, the temperature of the Si gradually drops to room temperature when the pulsed irradiation is stopped. At this time, the once-melted silicon solidifies to yield a polycrystalline state. The cooling process depends on the thermal conductivity of the base gate electrode. As shown by curve (1), the temperature of the silicon sharply drops when the gate electrode is made from a conventional single-layer metal film. On the other hand, as shown by curve (3), silicon on an insulating substrate made from glass or the like cools relatively slowly. This is because the thermal conductivity of glass is lower than that of metal, etc. Curve (2) represents the cooling curve when the top layer of the gate electrode is constructed from a material with relatively low thermal conductivity, according to this invention. As is clear from the graph, this cooling curve (2) is close to cooling curve (3). In other words, with this invention, the time difference from melting to solidifying for silicon on glass and silicon on a gate electrode can be minimized. Thus, silicon of a nearly uniform crystal state can be obtained regardless of differences in the bases, making it easy to optimize the laser annealing parameters.

[0020]

Figure 4 is a process diagram showing another application example of a gate electrode 5 formation method. As shown in (A), a metal film that will form the bottom layer 5b is sputtered onto an insulating substrate 1 made from glass or the like. For example, Ti is formed as the metal film to a thickness of 200 nm. Next, as shown in (B), the bottom layer 5b is patterned into the shape of the gate electrode. Then, as shown in (C), the surface of the bottom layer 5b is reformed to provide a top layer 5a. In other words, a top layer 5a made from TiN is formed by heat treating the bottom layer 5b in a nitrogen atmosphere. Thus, a gate electrode 5 can be obtained with a multilayered structure laminating a top layer 5a and a bottom layer 5b. The process thereafter is the same as that in Figure 2.

[0021]

Figure 5 is a schematic, partial cross-sectional drawing showing a second condition of embodiment of the thin film semiconductor device of this invention. For the sake of simplicity,

reference numbers correspond to parts that correspond to the first embodiment shown in Figure 1. In this condition of embodiment also, a thin film transistor 3 with a bottom-gate structure, in which a gate electrode 5, an insulating film 4, and a semiconductor thin film 2 are laminated in order from the bottom up, is formed accumulated on an insulating substrate 1. As a characteristic item, a thermally conductive base film 20 is formed on the surface of the insulating substrate 1, made from glass or the like, adjacent to the gate electrode 5 when viewed from the top, to even out the thermal conductivity of the surface of the insulating substrate 1. In this connection, the gate electrode 5 is a single-layer metal film of Cr, Mo, or Ta, or the like. On the other hand, the base film 20 is made from a transparent conductive film of ITO, or the like. The semiconductor thin film 2 possesses a polycrystalline structure that has been recrystallized by energy irradiation of, e.g., laser light, in a state extending over the gate electrode 5 and base film 20 with an interceding insulating film 4. As described above, when the semiconductor thin film 2 is recrystallized by laser annealing in a bottom gate thin film transistor, in this condition of embodiment, a base film 20 with greater thermal conductivity than glass is provided surrounding the gate electrode in order to make thermal distribution more uniform. Thus, a good-quality polycrystalline structure can be obtained.

[0022]

Figure 6 is a schematic, oblique-view drawing showing an example of an active matrix liquid crystal display device in which a thin film semiconductor device of this invention is assembled as a drive substrate. This display device is constructed with an electrooptical substance 50, made from liquid crystal or the like, held between a drive substrate 1 and an opposing substrate 60. A pixel array and peripheral circuits are formed accumulated on the drive substrate 1. The peripheral circuits are divided into a vertical scanning circuit 41 and a horizontal scanning circuit 42. In addition, terminal electrodes 47 are formed at the top edge of the drive substrate 1 for external connections. Each terminal electrode 47 is connected to the vertical scanning circuit 41 and a horizontal scanning circuit 42 by means of wiring 48. Intersecting gate wiring 43 and signal wiring 10 are formed in the pixel array. The gate wiring 43 is connected to the vertical scanning circuit 41 and the signal wiring 10 is connected to the horizontal scanning circuit 42. A pixel electrode 14 and the thin film transistor 3 that drives it is formed at the intersection of the two wiring [patterns] 43, 10. Meanwhile, a pair of electrodes, not shown, is formed on the inner surface of the opposing substrate 60.

[0023]
Effect

According to the first aspect of this invention, as described above, the gate electrode possesses a multilayered structure, in which a top layer with relatively low thermal conductivity and the electrical conductivity necessary to form contacts is laminated with a bottom layer with relatively high thermal conductivity and electrical conductivity necessary to function as wiring. With this structure, energy irradiation is received with a semiconductor thin film extending over the gate electrode and insulating substrate with an interceding insulating layer, making it possible to manifest a uniform and optimally recrystallized polycrystalline structure. In addition, with the second aspect of this invention, a thermally conductive base film is formed on the surface of the insulating substrate so as to be adjacent to the gate electrodes when viewed from the top, thereby evening out the thermal conductivity of the surface of the insulating substrate. The semiconductor thin film receives energy irradiation in a state extending over the gate electrode and insulating substrate with an interceding insulating layer, making it possible to manifest a uniform and optimally recrystallized polycrystalline structure.

Brief description of the figures

Figure 1 is a partial sectional drawing showing a first condition of embodiment of the thin film semiconductor device associated with this invention.

Figure 2 is a process diagram showing a method of manufacturing a first condition of embodiment.

Figure 3 is a graph showing the temperature changes in the semiconductor thin film during laser annealing treatment.

Figure 4 is a process diagram showing another example of a method of manufacturing a thin film semiconductor device of this invention.

Figure 5 is a partial sectional drawing showing a second condition of embodiment of the thin film semiconductor device associated with this invention.

Figure 6 is a schematic, oblique-view drawing showing an example of an active matrix display device assembled using the thin film semiconductor device of this invention.

Figure 7 is a graph comparing the reliability of bottom-gate thin film transistors with that of top-gate thin film transistors.

1 ... insulating substrate, 2 ... semiconductor thin film, 4 ... insulating film, 5 ... gate electrode, 7 ... source region, 8 ... drain region, 9 ... interstitial film, 10 ... signal wiring, 14 ... pixel electrode, 20 ... base film.

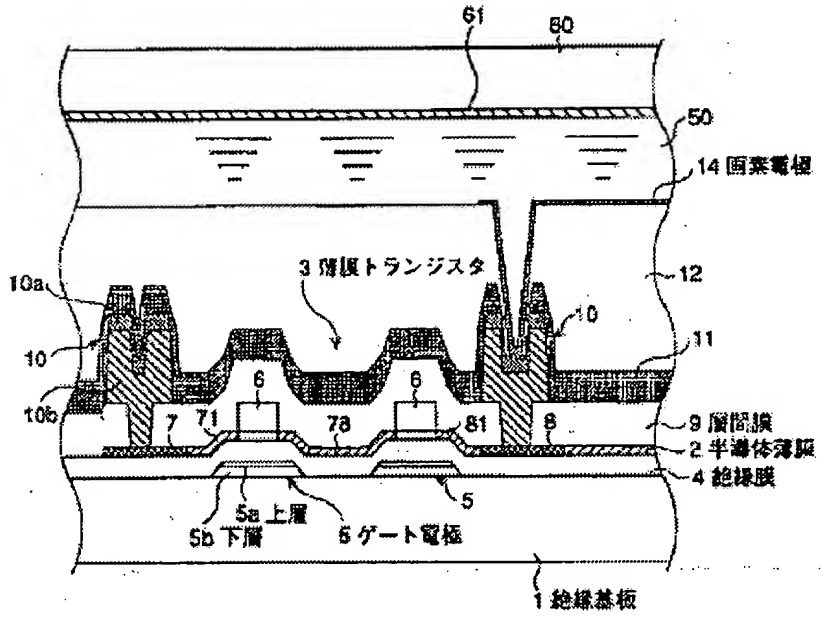


Figure 1

Key		
	1	Insulating substrate
	2	Semiconductor thin film
	3	Thin film transistor
	4	Insulating film
	5	Gate electrode
	5a	Top layer
	5b	Bottom layer
	9	Interstitial film
	14	Pixel electrode

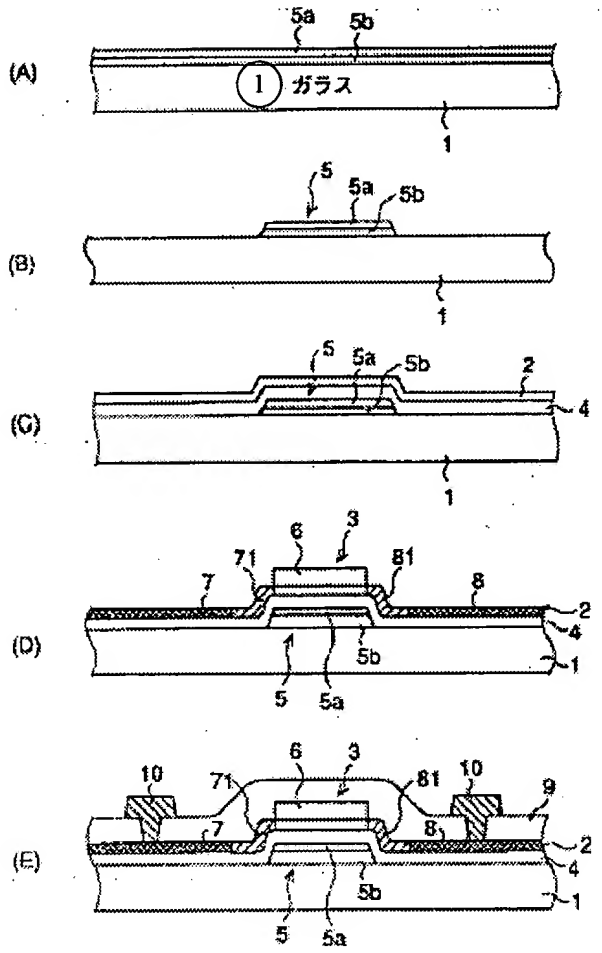


Figure 2

Key: 1 Glass

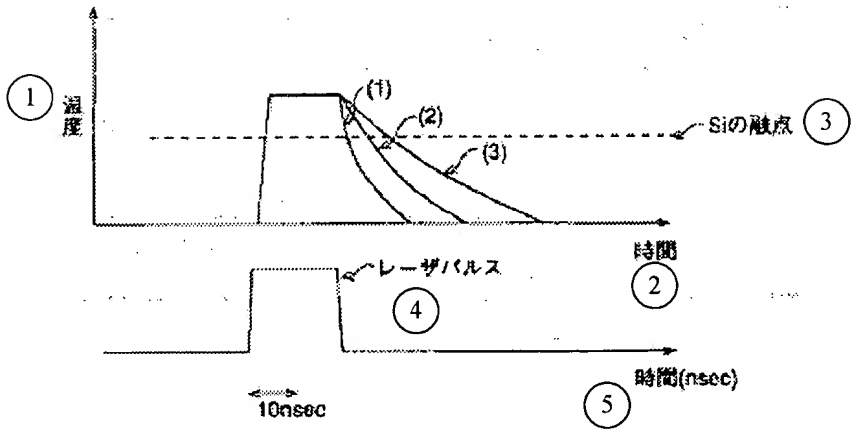


Figure 3

Key: 1 Temperature
2 Time

3 Melting Temperature of Si
4 ← Laser Pulse
5 → Time (nsec)

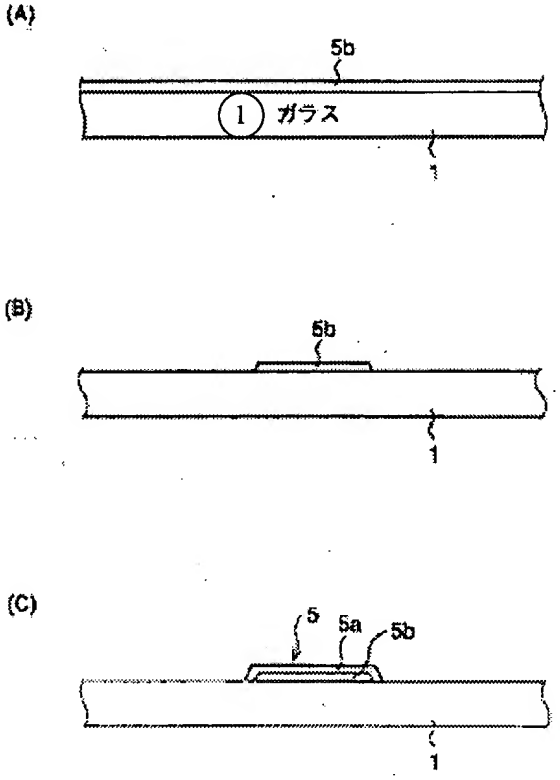


Figure 4

Key: 1 Glass

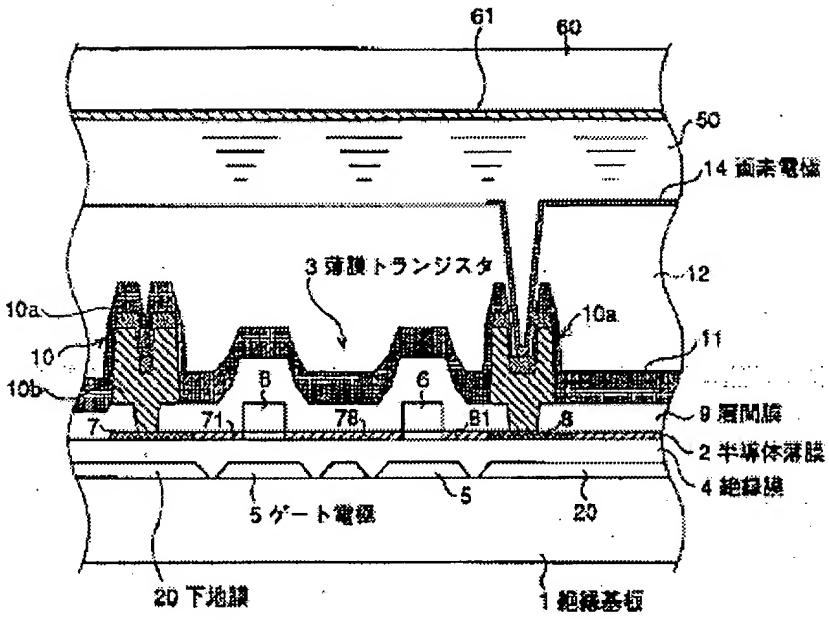


Figure 5

Key:
1 Insulating substrate
2 Semiconductor thin film
3 Thin film transistor
4 Insulating film
5 Gate electrode
9 Interstitial film
14 Pixel electrode
20 Base film

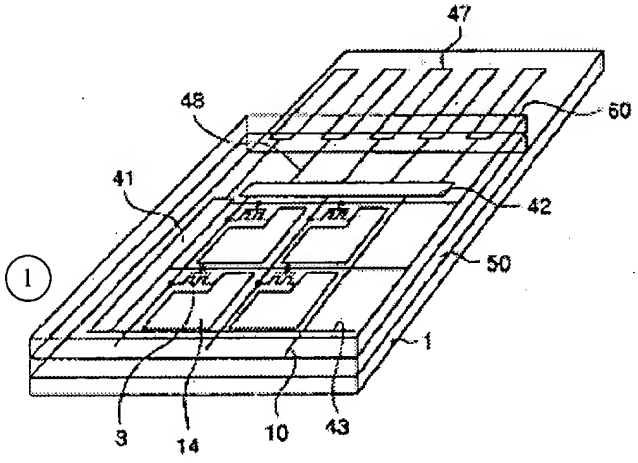


Figure 6

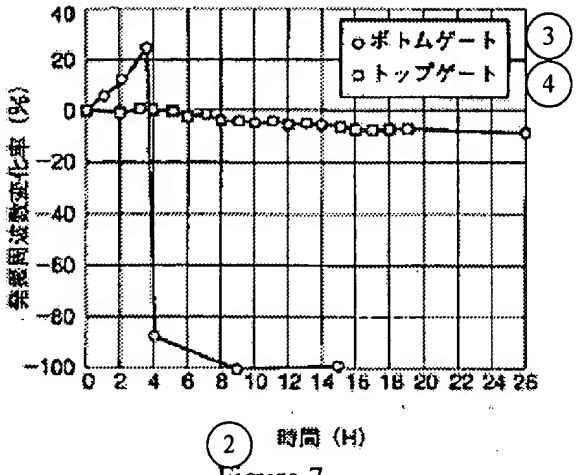


Figure 7

Key: 1 Oscillation frequency variation rate
2 Time (h)
3 Bottom gate
4 Top gate